Department of Physics Nirmala College Muvattupuzha

Laboratory Manual for BSc. Physics Model 2 (Semester 2)

Applied electronics

2017-2020

Compiled and Edited

by

Dr. Aloysius Sabu N

Associate Professor of Physics

1. Characteristics of Junction Field Effect Transistor (JFET)

Aim:
To study the Drain and Transfer Characteristics of a Junction Field Effect Transistor (JFET).
Components:
JFET (BFW10), Bread board, Regulated Power supply (0 - 2 V) and (0 - 12 V), Ammeters (0 - 20 mA), Voltmeter V_1 (0 - 2V), Voltmeter V_2, (0 - 10V), Connecting wires (Single Strand)
Theory and Operation:

1. Drain characteristics are obtained between the drain to source voltage ($\mathbf{V_{DS}}$) and drain current ($\mathbf{I_D}$) taking gate to source voltage ($\mathbf{V_{GS}}$) as the constant parameter.
2. Transfer characteristics are obtained between the gate to source voltage ($\mathbf{V_{GS}}$) and drain current ($\mathbf{I_D}$) taking drain to source voltage ($\mathbf{V_{DS}}$) as the constant parameter.

FET Parameters

1. **Drain Resistance ($\mathbf{r_d}$):** It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region.

$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at a constant $\mathbf{V_{GS}}$ (from drain characteristics)

2. **Trans Conductance ($\mathbf{g_m}$):** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant $\mathbf{V_{DS}}$.

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant $\mathbf{V_{DS}}$ (from transfer characteristics).

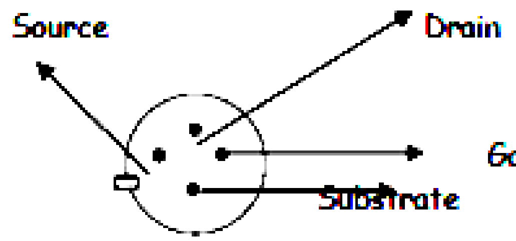
The value of g_m is expressed in mho's (℧) or Siemens (**s**).

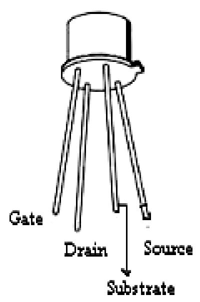
3. **Amplification factor (µ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).

$$\boldsymbol{\mu} = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) \times \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

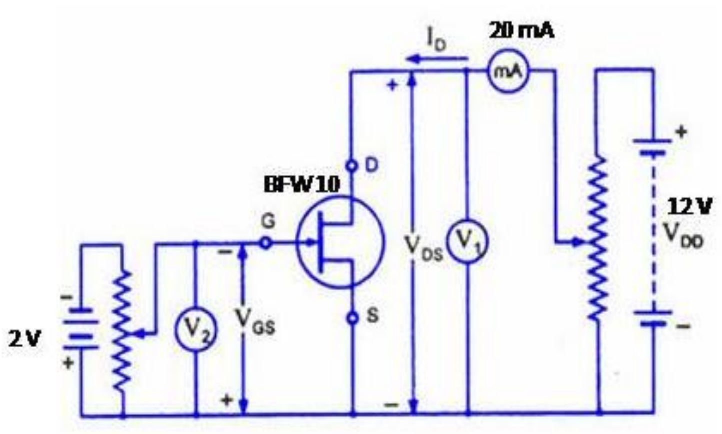
$$ie.\ \boldsymbol{\mu} = \boldsymbol{r_d} \times \boldsymbol{g_m}$$

Pin assignment of FET:





Circuit Diagram:



Procedure:

Drain Characteristics:

1. Connect the circuit as shown in the figure1.
2. Keep $\mathbf{V_{GS} = 0V}$ by varying $\mathbf{V_{GG}}$.
3. Varying $\mathbf{V_{DD}}$ gradually in steps of **1V** up to **10V** note down drain current $\mathbf{I_D}$ and drain to source voltage ($\mathbf{V_{DS}}$).
4. Repeat above procedure for $\mathbf{V_{GS}}$ = **-0.4, -0.8, -1.2** and **-1.6 V**

Transfer Characteristics:

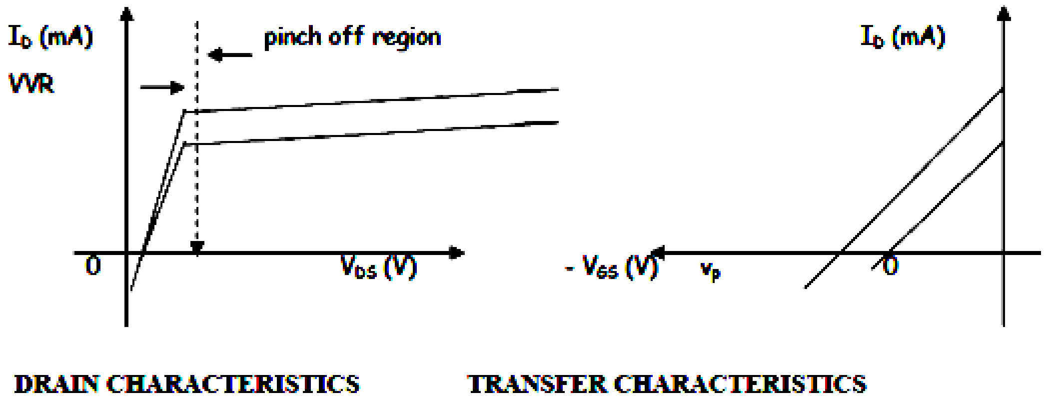
1. Connect the circuit as shown in the figure1.
2. Set voltage $\mathbf{V_{DS} = 4V/8V}$
3. Varying $\mathbf{V_{DS}}$ in steps of 0.5V until the current $\mathbf{I_D}$ reduces to minimum value.
4. Varying $\mathbf{V_{GG}}$ gradually, note down both drain current $\mathbf{I_D}$ and gate-source voltage ($\mathbf{V_{GS}}$).
5. Repeat above procedure (step 3) for $\mathbf{V_{DS}}$ = 4V/ 8V

Observations:

Drain Characteristics						
V_{DS} (Volts)	**V_{GS} = 0V**		**V_{GS} = -0.4V**		**V_{GS} = -0.8V**	**V_{GS} = -1.2V**
	V_{DS}(Volts)	**I_D(mA)**	**V_{DS}(Volts)**	**I_D(mA)**	**V_{DS}(Volts)**	**I_D(mA)**
0						
2						
4						
6						
8						
10						

Transfer Characteristics			
V_{DS} = 4V		**V_{DS} = 8V**	
V_{GS}(Volts)	**I_D(mA)**	**V_{GS}(Volts)**	**I_D(mA)**
0			
0.5			
1.0			
1.5			

Graph:



1. Plot the drain characteristics by taking $\mathbf{V_{DS}}$ on X-axis and $\mathbf{I_D}$ on Y-axis at a constant $\mathbf{V_{GS}}$.
2. Plot the transfer characteristics by taking $\mathbf{V_{GS}}$ on X-axis and taking $\mathbf{I_D}$ on Y-axis at constant $\mathbf{V_{DS}}$.

Calculations from Graph:

1. **Drain Resistance (r_d):**
   $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at a constant $\mathbf{V_{GS}}$ (from drain characteristics)
2. **Trans Conductance (g_m):**
   $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant $\mathbf{V_{DS}}$ (from transfer characteristics).

   The value of $\mathbf{g_m}$ is expressed in mho's (℧) or Siemens (**s**).

3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).
   $$\boldsymbol{\mu} = \left(\frac{\boldsymbol{\Delta V_{DS}}}{\boldsymbol{\Delta I_D}}\right) \times \left(\frac{\boldsymbol{\Delta I_D}}{\boldsymbol{\Delta V_{GS}}}\right) = \frac{\boldsymbol{\Delta V_{DS}}}{\boldsymbol{\Delta V_{GS}}}$$
   $$ie.\ \boldsymbol{\mu} = \boldsymbol{r_d} \times \boldsymbol{g_m}$$

Result: Drain and Transfer characteristics of a FET are studied.

Outcomes: Students are able to

1. Analyze the Drain and transfer characteristics of FET in Common Source configuration.
2. Calculate the parameters transconductance (g_m), drain resistance ($\mathbf{r_d}$) and amplification factor (**μ**).

2. Characteristics of Uni-Junction Transistor (UJT)

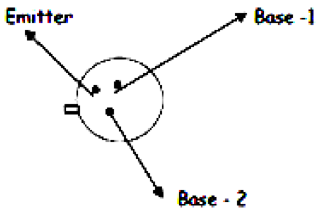
Aim:

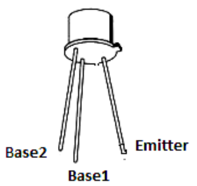
To study and plot the characteristics of UJT

Components: UJT 2N 2646, Resistors (1 K ohm), Bread board, Regulated Power supply (0 - 2 V) and (0 - 12 V), Ammeters (0 - 20 mA), Voltmeter (0 - 2V), Voltmeter (0 - 10V), Connecting wires (Single Strand)

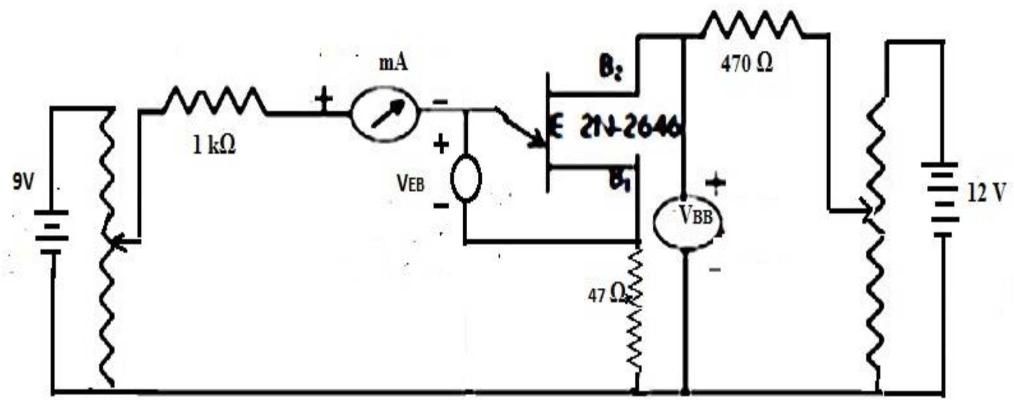
Pin assignment of UJT:

The UJT- junction is a 3 - terminal solid-state device (emitter and the two bases)



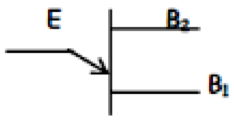


Circuit Diagram:

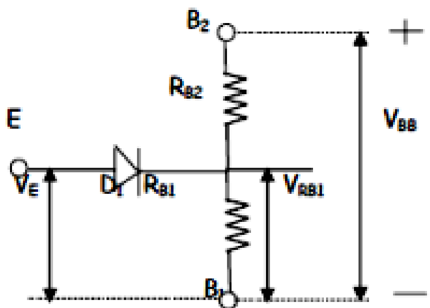


Operation:

. The simplified equivalent circuit is shown below:



Symbol of UJT



Equivalent Circuit

Referring to equivalent circuit:

1. When no voltage is applied between B_1 and B_2 with emitter open, the inter base resistance is give by $R_{BB} = R_{B1} + R_{B2}$.
2. When a voltage V_{BB} is applied between B_1 and B_2 with emitter open, voltage will divide up across R_{B1} and R_{B2}.

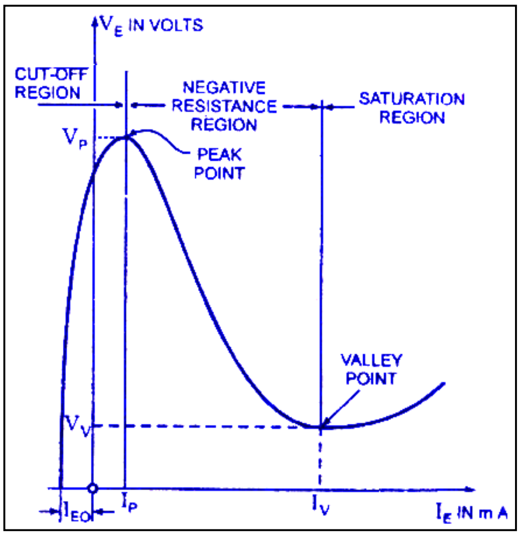
$$V_{R_{B_1}} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \times V_{BB}$$

$$\frac{V_{R_{B_1}}}{V_{BB}} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \times V_{BB}$$

$$V_{R_{B_1}} = \eta V_{BB},$$

where the intrinsic stand-off ratio

$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$



The typical value of η ranges from 0.56 to 0.75.

The potential drop ηV_{BB} across R_{B_1} reverse biases the diode thereby dropping the emitter current to zero. Here, up to the peak point, the diode is reverse biased and hence, the region to the left of the peak point is called cut-off region. When emitter voltage V_E equals the peak voltage $V_P = \eta V_{BB} + V_D$, the diode starts conducting and holes are injected into n-layer. Hence, resistance decreases thereby decreasing V_E for the increase in I_E. So there is a negative resistance region from peak point P to valley point V.

After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN-junction diode. The region to the right of the valley point is called saturation region.

In the valley point, the resistance changes from negative to positive. The resistance remains positive in the saturation region.

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Set output voltage V_{BB} = 8V by varying V_{BB}.
3. Varying V_{EE} gradually, note down both emitter current I_E and emitter voltage (V_E).
4. Step size is not fixed because of non linear curve. Initially Vary V_{EE} in steps of 1V. Current I_E remains zero. As voltage is varied further, current starts increasing while voltage V_E drops. Note down the readings V_E and I_E.
5. Repeat above procedure (step 3) for V_{BB} = 10V.
6. Plot the tabulated readings on a graph sheet with I_E on X-axis and V_E on Y-axis.

Observations:

V_{BB} = 8V		**V_{BB} = 10V**	
I_E(mA)	V_E(V)	I_E(mA)	V_E(V)

Inference:

1. There is a negative resistance region from peak point to valley point.
2. Increase in V_{BB} increases the value of peak and valley voltages.

Result:

The emitter characteristics of UJT are studied.

a. Peak Voltage, V_p ____________ Volts.
b. Valley Voltage, V_v ____________ Volts.
c. Valley Current, I_v ____________ mA.
d. Negative Resistance ____________ Ohms
e. Intrinsic stand-off ratio η -----------------

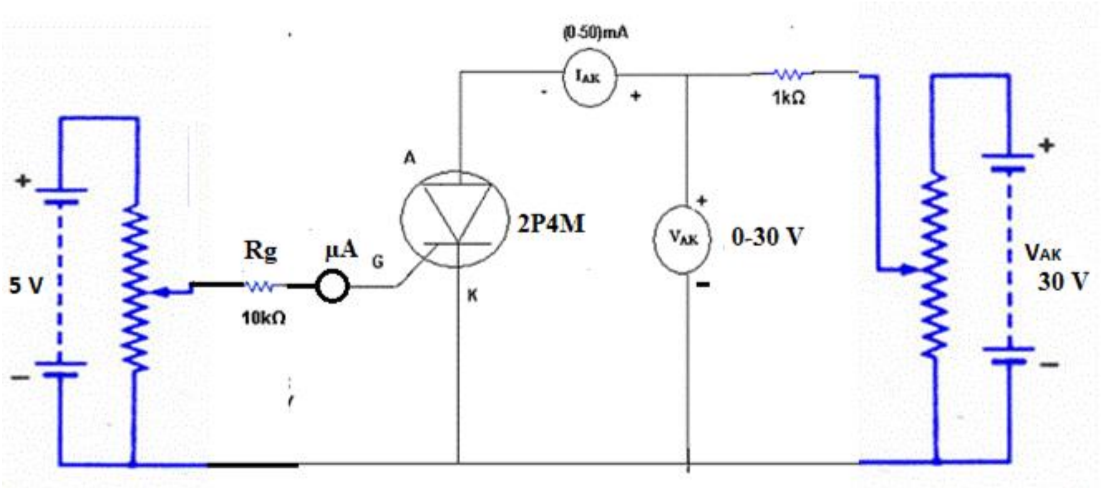
Outcome: Students are able to obtain the Emitter characteristics of UJT
Students are able to appreciate the invention of UJT

3. V-I Characteristics of Silicon controlled rectifier (SCR)

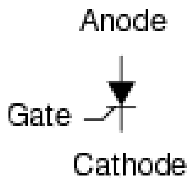
Aim: To draw the V-I Characteristics of Silicon controlled rectifier.

Apparatus: SCR (2P4M), Regulated Power Supplies (0-2V) and (0-12V), Resistors 10kΩ, 1kΩ, Ammeter (0-20) mA, Voltmeter (0-12V), Breadboard and Connecting Wires.

Circuit Diagram:



Symbol of SCR



Theory:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1, J_2, J3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cut off. When anode voltage is increased J_2 tends to breakdown.

When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased. Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increases in extremely small current, junction J_2 break down and SCR conducts heavily.

When gate is open the break-over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

Procedure:

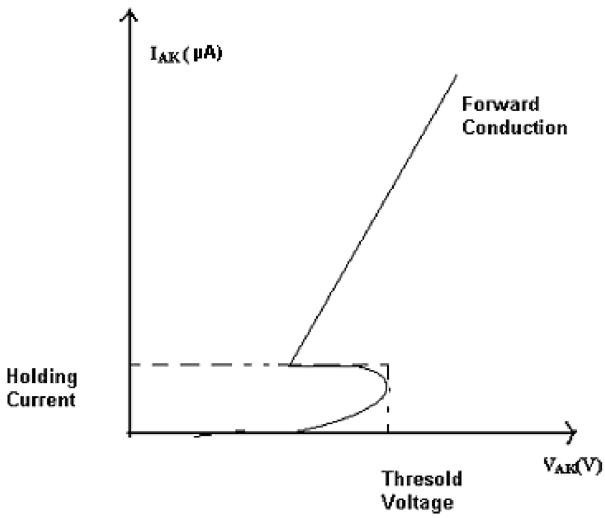
1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter. Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK}.

Observation:

Ig =	**(µA)**
V_{AK}(V)	**I_{AK} (mA)**

Ig =	**(µA)**
V_{AK}(V)	**I_{AK} (mA)**

Model Wave form:



Result: SCR Characteristics are observed.

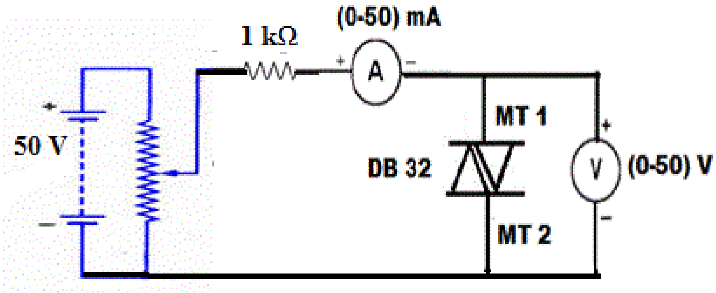
OUTCOME: Students are able to obtain the Emitter characteristics of SCR

4. Characteristics of a DIAC

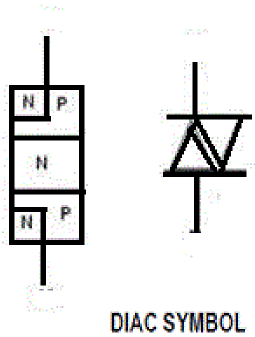
AIM: To plot the VI characteristics of a DIAC

APPARATUS REQUIRED: DIAC (DB 32), power supply (50 V), DMM, Bread board Connecting wires (Single Strand)

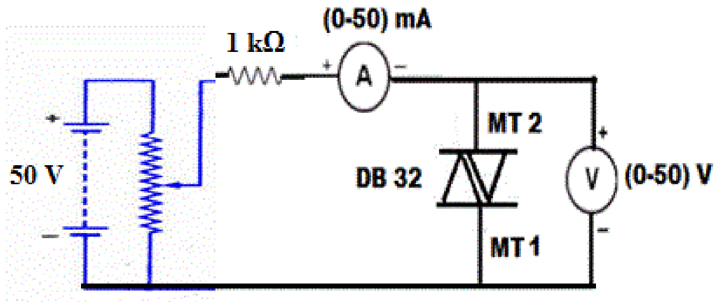
THEORY:DIAC is a diode that can work on AC. The DIAC has symmetrical breakdown characteristics. The leads are interchangeable. It turns on around 32V. While conducting, it acts like a low resistance with a drop of around 3V. When not conducting, it acts like an open switch.



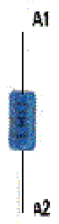
FORWARD BIAS



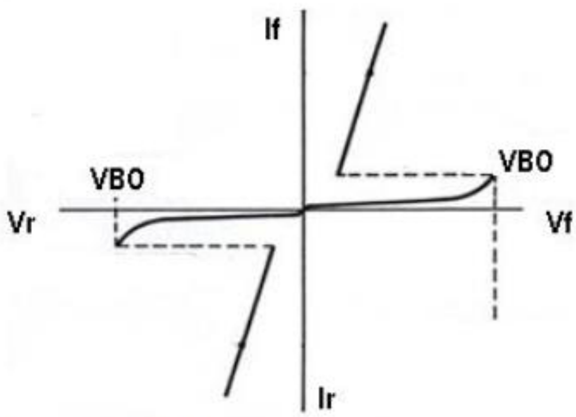
DIAC SYMBOL



REVERSE BIAS



DIAC COMPONENT VIEW



PROCEDURE:

1. Connect the circuit as per the circuit diagram.

2. Change the voltage in steps till 32V and observe Voltmeter reading and Ammeter reading. Note the start of break overvoltage. Observe the conduction of DIAC..

3. Now change the DIAC direction and vary the voltage insteps in the negative direction till -32V and Observe Voltmeter reading and Ammeter reading. Note the start of break overvoltage. Observe the conduction of DIAC.

.4. The characteristics are tabulated and plotted.

OBSERVATIONS:

Forward Characteristics		Reverse Characteristics	
V_f (V)	I_f (mA)	V_r (V)	I_r (mA)

RESULT: The VI characteristics of a DIAC have been plotted.

OUTCOME:

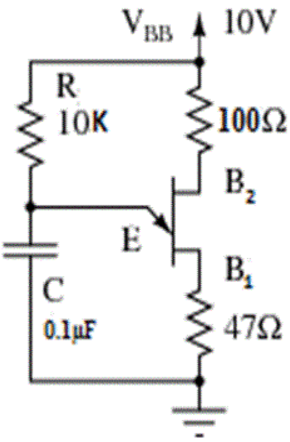
- Students acquire skill in connecting components using breadboard and connecting wires to form circuit.
- They become able to determine the Emitter characteristics of SCR

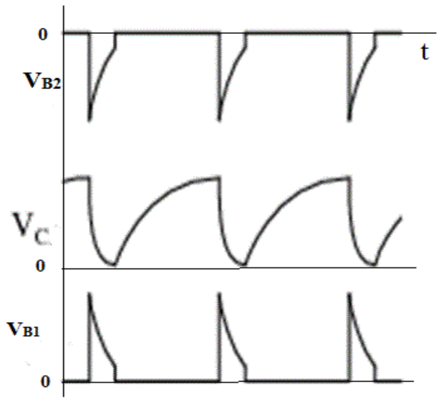
5. UJT as a Relaxation Oscillator

Aim: To Study the operation of UJT as a Relaxation Oscillator

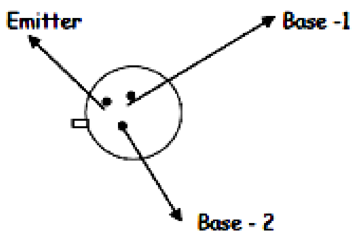
Apparatus: UJT (2N2646), CRO (0 – 20 MHz (Dual channel), Function generator 1Hz – 1 MHz, Capacitor (0.1µF), Resistors (100Ω, 47Ω, 10 kΩ), Bread board and connecting wires, Regulated Power supply 0-12V DC

Circuit diagram:





Pin assignment of UJT:



Viewing from the side of pins

Frequency of oscillations:

The time period and hence the frequency of the saw-tooth wave can be calculated as follows:

$$\mathbf{T} = \boldsymbol{RClog_e}\left(\frac{1}{1-\eta}\right)$$

$$= \mathbf{2.303}\boldsymbol{RClog_{10}}\left(\frac{1}{1-\eta}\right)$$

If the discharge time of the capacitor is neglected, then t = T, the period of the wave. Therefore, frequency of oscillations of saw-tooth wave,

$$\boldsymbol{f} = \frac{\mathbf{1}}{\boldsymbol{T}} = \frac{\mathbf{1}}{\mathbf{2.303}\boldsymbol{RClog_{10}}\left(\frac{1}{1-\eta}\right)}$$

Design

From the data sheet of UJT 2N2646,
η = 0.56 to 0.75, Typical value of η = 0.6, V_V = 1.5 V, I_P= 5 µA and I_V= 4 mA
$V_P = \eta V_{BB} + V_D$ = (0.6 x 9) + 0.7 = 6.1 V

$$R_{max} = \frac{V_{BB} - V_P}{I_p} = \frac{9 - 6.1}{5\mu A} = \frac{2.9}{5}\ M\Omega = 0.58M\Omega$$

$$R_{min} = \frac{V_{BB} - V_v}{I_V} = \frac{9 - 1.5}{4mA} = \frac{7.5}{45}\ k\Omega = 1.875\ k\Omega$$

Taking geometric mean,
$R = \sqrt{R_{max} \times R_{min}} = \sqrt{(0.58M\Omega} \times 1.875\ k\Omega) = 32.76$ kΩ
Select, R= 33 kΩ. For convenience select R= 10 kΩ
Let the required frequency be 1 kHz, then T=1/f =10^{-3}s.

$$T = RC\log_e\left(\frac{1}{1-\eta}\right)$$

$$10^{-3}s = 10x10^{3}xC\ \log_e\left(\frac{1}{1-0.6}\right)$$

$$C = \frac{10^{-7}}{\log_e\left(\frac{1}{1-0.6}\right)} = \frac{10^{-7}}{0.9163} = 0.1\mu F$$

Procedure:

1. Connect the circuit as shown in figure.
2. Apply 10 V DC power supply to the circuit.
3. Observe the output waveform on the CRO at B1, B2 and V_O and Plot the graphs
4. Vary the time constant (RC) by varying capacitor (C) or potentiometer (R) and observe the variations in the output pulses on the CRO at B1, B2 and V_O.

Result:

UJT relaxation oscillator is constructed and output waveforms are obtained.
Frequency of oscillations = -------Hz.

Outcome:

- After finishing this experiment students are able to understand the operation of UJT as a relaxation oscillator.
- Students become able to design a relaxation oscillator

6. JFET common source amplifier

Aim:

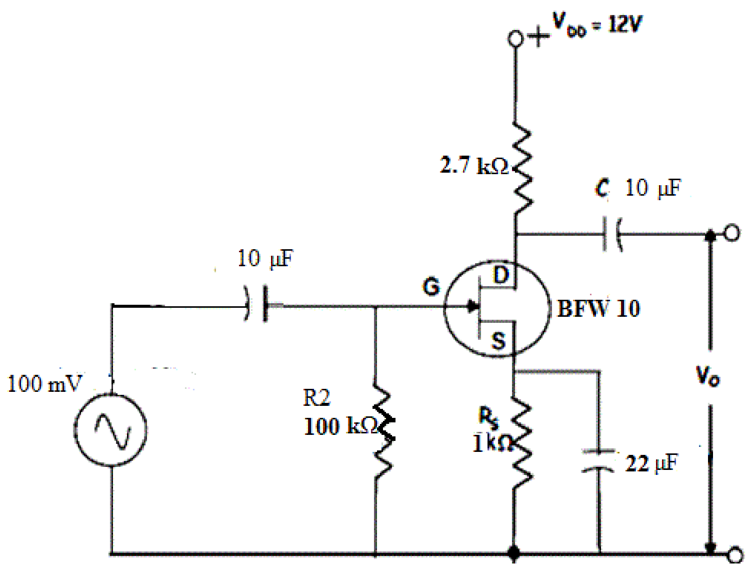
To study the JFET common source amplifier and find it’s cut off frequencies and Bandwidth.

Components: JFET BFW 10, Resistor 2.7KΩ, 1.0 KΩ, 100 KΩ, Capacitor 10µF, 22µF, Bread Board, power supply, Function Generator, Connecting Wires.

Theory:

The JFET is a unipolar voltage controlled device. The drain current is controlled by the voltage applied at the gate. In the circuit shown self bias maintains drain current and mutual conductance g_m relatively constant. Constant g_m results a constant voltage gain. The reverse biased junction provides high input impedance.

Circuit Diagram:



Procedure:

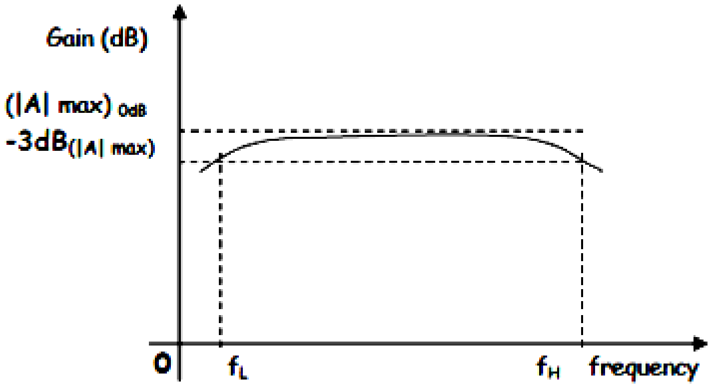
1. Connect the circuit as shown in the circuit diagram.
2. Set source voltage V_S = 50mV (say) at 1 KHz frequency using the function generator.
3. Keeping input voltage constant vary the frequency from 50 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) verses Frequency on a semi log graph sheet.
5. Calculate the bandwidth from the graph.
6. Calculate all the parameters at mid band frequencies (i.e. at 1 KHz).
7. To calculate voltage gain

$$\text{Gain A} = \frac{\text{Output Voltage}}{\text{InputVoltage}} = \frac{V_o}{V_i}$$

$$\text{Gain in (dB)} = 20 \log (Vo/Vi)$$

Expected waveform:

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as $f_L$and f_H and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut off and lower cut off frequency is referred to as bandwidth (f_H - f_L).



Observation tables:

V_i = 50mV

Frequency	Vo(volts)	Gain= Vo/Vs	Gain(dB)=20 log(Vo/Vs)

Lower cut-off frequency (f_L) =

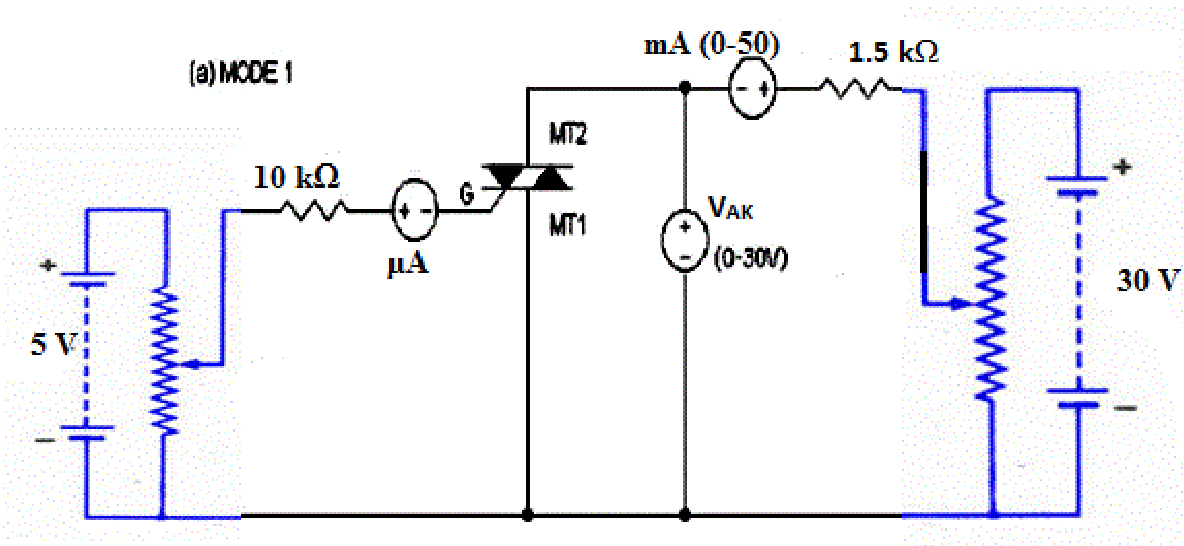
Upper cut-off frequency (f_H) =

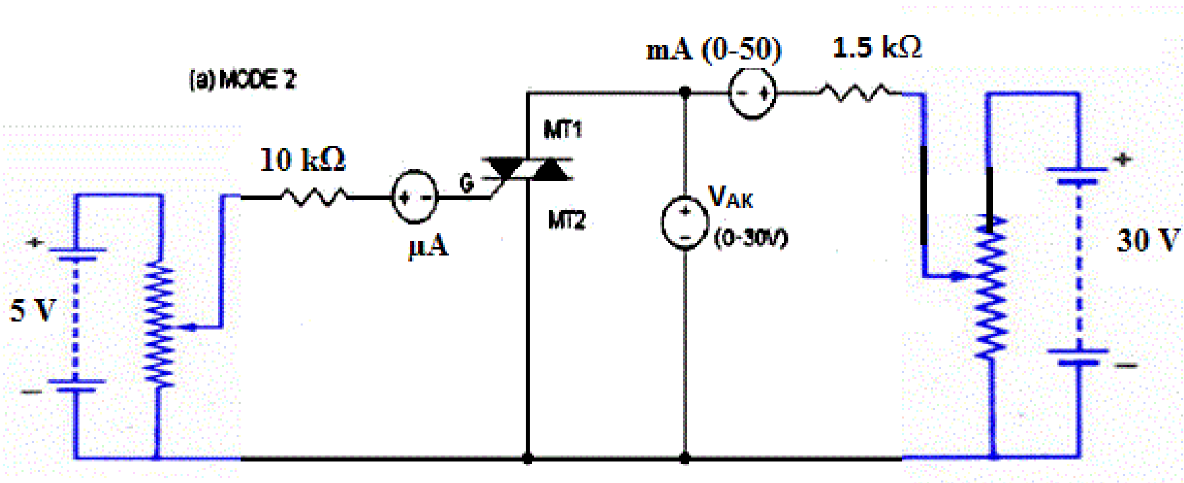
Bandwidth β = f_H - $f_{L=}$

Result:
JFET common source amplifier is studied and it's cut off frequencies and Bandwidth is found.
Outcome:
Students are able to determine the bandwidth of common source JFET amplifier.

7. V-I Characteristic of TRIAC

Aim: - To study V-I characteristic of TRIAC.
Apparatus: - TRIAC BT 136, Circuit board 0-300V high voltage supply, 0-30V low voltage supply, Ammeter (0-10mA, 0-1A), voltmeter (0-250V), Resistor 10KΩ, 1.5 KΩ connecting wires
Circuit Diagram





Theory: A TRIAC is a device which can be turned on through the gate pulse for both positive and negative values of VAK and turned off using power circuit i.e., turn on is controlled but turn off is uncontrolled in a TRIAC. The voltage at which the TRIAC gets into conduction state is called forward breakover voltage (V_{BO}) for positive voltages and reverse break over voltage (V_{BR}) for negative voltages. If the gate current is increased then the forward break over and reverse break over voltages will be reduced. The current at which the TRIAC turns on is called latching current (IL). Once the TRIAC is turned on, no need of the gate pulse i.e., gate pulse can be removed once the device is turned on. The minimum current required for the device to keep the thyristor on is holding current (IH). The ratio of latching to holding currents will be 3-5. When the gate current is increased, the break over voltage values will be reduced.

Procedure:

Mode 1

1. Connect the circuit as per the connection diagram.
2. Keep the gate current a fixed value (Ig1).
3. By varying the anode to cathode voltage note the voltage (Vak) and current (Ia).
4. Note the forward break over voltage (VBO), latching current (IL) and holding current(IH).
5. Change the gate current value (Ig2, Ig3) and repeat steps 3 and 4.

6. Plot the graph between V_{AK} and I_A, denoting IL, IH, and VBO's.

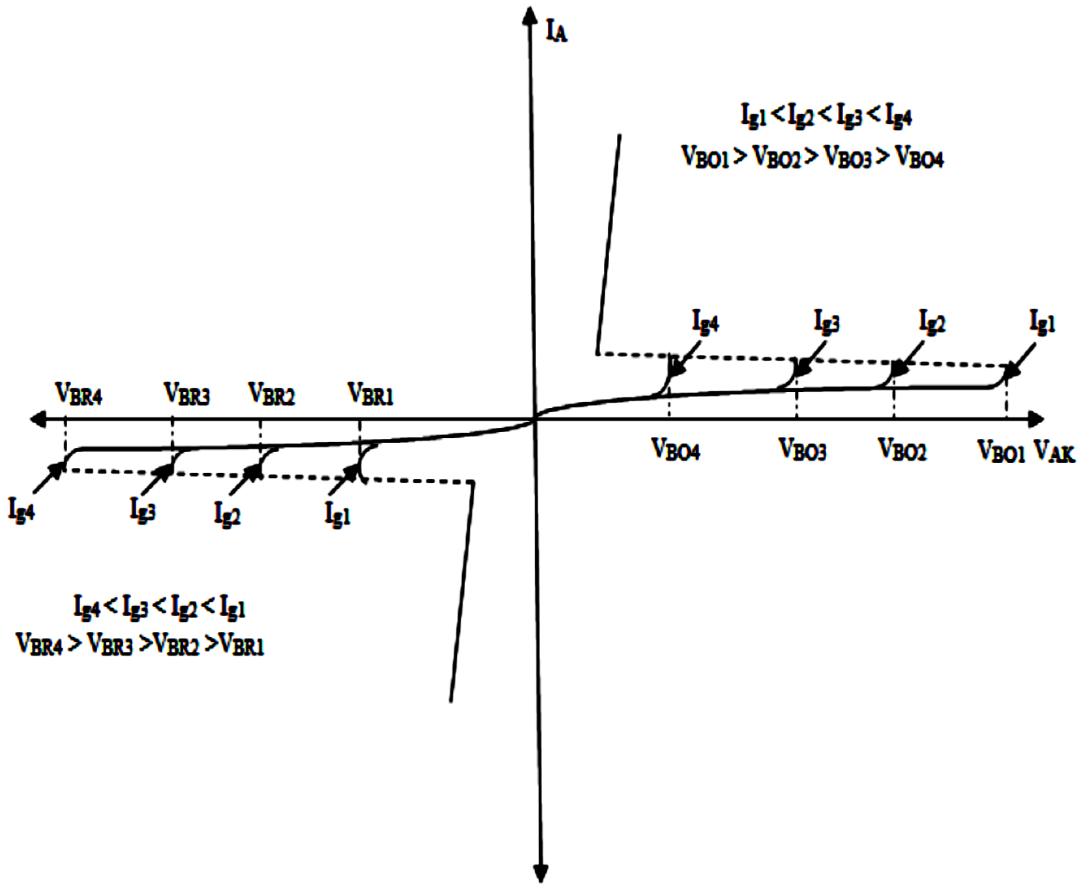
Mode 2

Connect are made as shown in circuit diagram. 2 Step no. S 2, 3, 4,5 and 6 are to be repeated as in mode 1.

Precautions:

1. While changing the gate current, first make the V_{AK} equal to zero and then vary I_g.

Model Graph:



Ig =	(μA)	Ig =	(μA)
V_{AK}(V)	I_{AK} (mA)	V_{AK}(V)	I_{AK} (mA)

Ig =	(μA)	Ig =	(μA)

Result:

Characteristics of TRIAC are studied for two different triggering currents.

Outcome

Students are able to understand the working principle of a TRIAC